Claims 1-44 are pending in this application. Claims 23-44 stand withdrawn from consideration. Claims 1, 2, 4, and 11 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent 5,818,069 to Kadosh et al. (herein "Kadosh"). Claims 1, 2, 6-8, 12, 13, and 17-19 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent 5,693,975 to Lien. Claims 12, 13, 15, and 22 were rejected under 35 U.S.C. § 102(b) as anticipated by U.S. patent 5,573,969 to Kim. Claims 3, 5, 9, 10, 14, 16, 20, and 21 were objected to as dependent upon rejected base claims, but were noted as allowable if rewritten in independent form to include all of the limitations of their base claims and any intervening claims.

Initially, applicants gratefully acknowledge the early indication of the allowable subject matter of claims 3, 5, 9, 10, 14, 16, 20, and 21.

Addressing now the rejection of claims 1, 2, 4, and 11 under 35 U.S.C. § 102(b) as anticipated by Kadosh, that rejection is traversed by the present response.

It is initially noted that claim 1 is amended by the present response to clarify features recited therein. Specifically, claim 1 recites a first semiconductor substrate, first and second transistors, each having a gate electrode and a pair of active regions, the pair of active regions formed in the semiconductor substrate, an isolation region, at least one slit formed in a top region of the isolation region, a conductive layer, and an interconnect layer having a top surface that is lower than a top surface of the gate electrode.

The features clarified in claim 1 are supported by the original specification, for example in Figure 3. With reference to Figure 3 as a non-limiting example as an embodiment of the present invention, a semiconductor device includes a semiconductor substrate 11, first and second transistors 15, 16 formed in the semiconductor substrate 11, and an isolation region 14 isolating the first and second transistors 15, 16 from each other. Further, one of the active regions of the first and second transistors 15, 16 are connected to each other by a

portion 22c of an interconnect layer 22, and that interconnect layer 22 has a top surface that is lower than a top surface of a gate electrode 18.

The above-noted structure is believed to clearly distinguish over the teachings in Kadosh.

Kadosh discloses, for example in Figures 5 and 11, that active regions of a first transistor 54 are formed in a substrate 52, while active regions of a second transistor 80 are formed in a second substrate 72 that is formed on the substrate 52 interposing an interlevel dielectric 66. In other words, in Kadosh the active regions of the first and second transistors 54, 80 are not formed in the same substrate.

As a result, Kadosh does not disclose or suggest an element equivalent to the claimed "isolation region" of claim 1.

Moreover, in Kadosh the interlevel dielectric 66 for isolating the first and second transistors 54, 80 from each other is not formed in the substrate 52. Further, in Kadosh the top surface of a conductive material 78 that connects the active regions of the first and second transistors 54, 80 is not positioned at a part lower than a top surface of a gate electrode 86 of the second transistor 80, again in contrast to claim 1 that specifically recites "the interconnect layer having a top surface which is lower than a top surface of the gate electrode".

Thereby, independent claim 1, and claims 2, 4, and 11 dependent therefrom, positively recite limitations neither taught nor suggested by Kadosh, and thus those claims distinguish over the teachings in Kadosh.

Addressing now the rejection of claims 1, 2, 6-8, 12, 13, and 17-19 under 35 U.S.C. § 102(b) as anticipated by Lien, that rejection is also traversed by the present response.

It is initially noted that independent claim 12 is similarly amended as in independent claim 1 noted above. Such structures are believed to distinguish over the teachings in Lien.

Lien does not disclose or suggest forming a slit in the top surface region of an isolation region 607. In Lien, the active regions 611a and 621a of first and second transistors are connected to each other by a p+ poly 611b and an n+ poly 621b formed on the isolation region.

In other words, Lien does not disclose or suggest either the "at least one slit formed in a top surface region of the isolation region" or the "conductive layer" recited in each of independent claims 1 and 12, and the claims dependent therefrom. Accordingly, each of the above-noted claims patentably distinguish over the teachings in Lien.

Addressing now the rejection of claims 12, 13, 15, and 22 under 35 U.S.C. § 102(b) as anticipated by Kim, that rejection is also traversed by the present response.

Kim discloses in Figure 3E a conductive wire 35 formed to fill a contact hole 7 on a well isolation 31, and the conductive wire 35 connecting active regions 15B and 25B of two transistors to each other.

However, Kim does not disclose or suggest the use of a "conductive layer formed on the inner walls of the slit" as positively recited in claim 12.

Moreover, in Kim the top surface of the conductive layer 35 is not positioned at a portion lower than a top surface of the gate electrode 4 of the transistors, in contrast to claim 12 that positively recites "the interconnect layer having a top surface which is lower than a top surface of the gate electrode".

In such ways, independent claim 12, and the claims dependent therefrom, patentably distinguish over the teachings in Kim.

As no other issues are pending in this application, it is respectfully submitted that the present application is now in condition for allowance, and it is hereby respectfully requested that this case be passed to issue.

Respectfully submitted,

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